TECHNOLOGY

Fully Self-Aligned High Speed Low Power MOSFET Fabrication

OVERVIEW

A new improvement in the high speed components for VLSI technologies is the vertical doping engineering (VDE), which resembles the SOI (Silicon On Insulator) technique in bulk Silicon. In a vertical engineering doped device, the junction capacitance of the device is reduced by decreasing its substrate doping level. In the meantime, a local heavily doped region is placed just beneath the channel region, which creates a rapidly changing vertical electric field and horizontal electron barrier to reduce the leakage current and to prevent punch-through effects. However, VDE structured fabrication technique is not well addressed. In current fabrication processes, it is often to have misalignment between heavily doped region and the gate, which will cause distortions and instability in performance. Another drawback of the existing technology is that, in e-beam lithography and broad beam implantation, it is difficult to control the doping profile due to mask wall scattering.

Researchers at the University of Maryland have developed new fabrication techniques for MOS/CMOS devices. Not only can the new techniques help optimize device fabrication process, but also it can reduce its processing steps, which could contribute to device manufacturing efficiency. In sub micron regime, the new technology will enable doping profile controllability and self-alignment between the heavily doped region and the gate. Compared with prior improvement attempts by scientists at Bell Labs, the new technology surpasses them in preserving device characteristics and simplifying fabrication processes.

See U.S. patent No. 6,309,934

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Additional Information

INSTITUTION

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PATENT STATUS

Patent(s) pending

LICENSE STATUS

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CATEGORIES

- Microelectronics

PS-96-038