TECHNOLOGY

A Power Constrained, High Performance, Multi-Rank DDRx SDRAM Scheduling Algorithm

OVERVIEW

Power consumption and heat dissipation considerations are constraining high performance DRAM memory systems just as they are constraining high performance processors. The combination of power limitation and data bus synchronization constraints will limit available memory bandwidth in DDR2 and future DDR3 SDRAM memory systems that do not adequately account for these bandwidth constraints.

Inventors at the University of Maryland have developed a DRAM command scheduling algorithm that achieves optimal bandwidth in short channel (2 rank) DDR2 and DDR3 memory systems.

As transistor budgets continue to grow, the trend toward multi-threaded cores and chip-level multiprocessors appears to be inevitable. Memory request streams from these processors will have higher access rates and less spatial locality compared to memory request streams from traditional uniprocessors. The higher access rate will require more bandwidth per pin from the memory system, and the decreased spatial locality property means an increase in the number of row cycles per transaction, even for open-page DRAM memory systems. Both effects of the multi-threaded and multi-processor system increase the importance of a low spatial locality and bandwidth optimized DRAM transaction and command scheduling algorithms such as the one proposed in this work.

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CATEGORIES

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EXTERNAL RESOURCES

- US Patent 7,543,102

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