TECHNOLOGY

Flexing Crossbars-Next Generation Packet Switches

OVERVIEW

Background:
Packet switching forms the core of nearly all traffic processing in IP and other data and multimedia networks and most networking infrastructures include a crossbar switch, an assembly of individual switches between multiple inputs and multiple outputs. Due to the need to handle transfer of data with higher efficiency and speed, there has been a significant interest in building packet switches on a chip.

Packet switching models that use a full crossbar switch overlook its high cross-point complexity and those that use multistage switching fabrics assume that the excessive routing time of such fabrics can be mitigated by parallel algorithms. However, neither assumption is realistic for on-chip realizations of packet switches. Packet switches using full crossbar architectures are not linearly scalable with respect to network size. The crosspoint complexity of full crossbar switch grows quadratically with their input size, and if such switches include internal buffers, their buffer space will also grow quadratically with their input size. These considerations make crossbar packet switching architectures impractical and not easily scalable in current FPGA and ASIC chips for more than a few tens of inputs.

Innovative Technology:
Researchers at the University of Maryland have invented a new packet switch model, called a flexing crossbar, to create a new parametric design space of packet switches and obtain high performance packet switches. The model has been designed to increase the throughput of the crossbars by using buffers within the neighborhood of the crosspoints. Flexing crossbars will likely overcome the scalability problem by injecting more sparsity to the grid fabric and lead to scalable congestion-free and distributed routing packet switching networks with significant potential impact on network servers and routers, making them both faster and their design and production more economical. The true worth of the flexing crossbar model is in its ability to represent a space of packet switches with sparse crossbar fabrics much the same way 3-stage Clos networks provide a design space of multistage non-blocking circuit switches. Extracting congestion-free packet switches from this space is just a matter of finding optimal combination of physical and performance metrics. The flexible crossbar chip will likely operate at the speed of the crosspoint and with buffering traffic can be pipelined to accomplish higher throughputs. All this will mean smaller latency and jitter, and faster traffic.

Advantages:

Applications:
-

APPLICATIONS

On-chip realization of packet switches

ADVANTAGES

Scalability
Congestion-free packet switching
Potential for faster networks and routers
Lower cost network servers and routers

CONTACT INFO

UM Ventures
0134 Lee Building
7809 Regents Drive
College Park, MD 20742
Email: umdtechtransfer@umd.edu
Phone: (301) 405-3947 | Fax: (301) 314-9502

Additional Information

INSTITUTION

University of Maryland, College Park

CATEGORIES

- Microelectronics
- Information Technology

EXTERNAL RESOURCES

PS-2014-004